What is Claimed is:

1. A pulse width position modulator, comprising:

a digital delay circuit receiving a native pixel clock and outputting multiple subclocks according to the native pixel clock, the multiple subclocks each skewed at different percentages of a native pixel clock period; and

a skew pulse generator receiving the multiple subclocks from the digital delay circuit and outputting multiple subpixels according to different combinations of the multiple subclocks thereby providing subpixel output resolution from the native pixel clock period.